PAL/NTSC COLOUR ENCODER

GENERAL DESCRIPTION

The TEA2000 is a monolithic integrated circuit, which encodes colour information and provides composite video output for driving a VHF or UHF modulator.

Features

- European PAL and American NTSC/M standard selectable
- Internal generation of burst timing and PAL-switch-function
- 6 bit binary TTL compatible input provides 64 different colours
- TTL compatible colour blanking input
- TTL compatible sync input

QUICK REFERENCE DATA

Supply voltage	V_{11-9}	typ.	12 V
Supply current at V_{11-9} = 12 V	I_{11}	typ.	55 mA
Input voltage pins 1,2,3,4,5,14,16,17,18	V_{IL}	max.	0,8 V
	V_{IH}	min.	2,0 V
Composite video output (sync tip to white)	$V_{6-9(p-p)}$	typ.	2,0 V
Operating temperature range	T_{amb}		0 to + 70 °C

PACKAGE OUTLINE

18-lead DIL; plastic with internal heat spreader (SOT-102H).

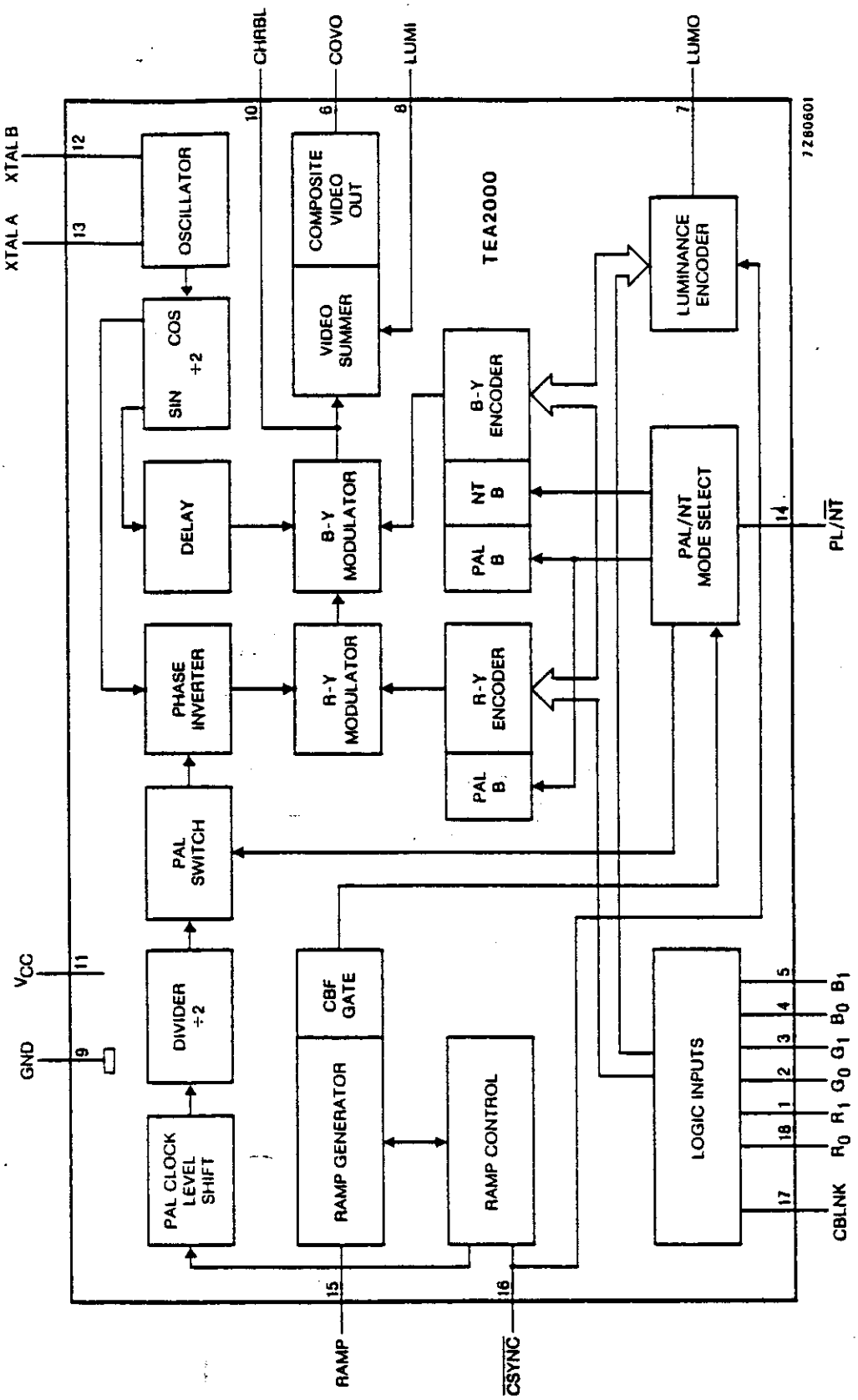

Fig. 1 Block diagram.

PINNING

1. Red 1 binary input
2. Green 0 binary input
3. Green 1 binary input
4. Blue 0 binary input
5. Blue 1 binary input
6. Composite video output
7. Luminance output to delay line
8. Luminance input from delay line
9. Ground 0 volt
10. Chrominance band limiting
11. Supply voltage
12. Oscillator inputs — 7,16 MHz crystal for NTSC
13. Oscillator inputs — 8,86 MHz crystal for PAL
14. PAL/NTSC switch
15. Ramp
16. Composite sync input ($\overline{\text{CSYNC}}$)
17. Composite blanking input (CBLNK)
18. Red 0 binary input

FUNCTIONAL DESCRIPTION

The TEA2000 PAL/NTSC colour encoder and video summer integrated circuit has an internal oscillator from which the (R-Y) and (B-Y) waveforms are generated. The TEA2000 accepts timing signals (composite sync, composite blanking) and a 6 bit binary coded input giving colour information. The inputs are organized as 2 bits per primary colour and gamma correction is applied to the resultant luminance and chrominance levels. Each of the equally spaced intensity levels (for each primary colour) is combined with those of the other primary colours. This produces 64 output colours comprising a wide range of saturated and desaturated colours, black, white and two levels of grey. The resultant output is a composite video signal compatible with the PAL and NTSC/M standards.

PIN DESCRIPTION

R0, R1, G0, G1, B0, B1, pins 18, 1,2,3,4 and 5.
These are the red, green and blue logic inputs. 2 bits per primary colour. These inputs are TTL compatible.

$\overline{\text{CSYNC}}$, pin 16.

Composite sync input requiring a negative logic signal, TTL compatible. For PAL operation the field sync must include line sync information.

XTALA, XTALB, pins 12 and 13.

Oscillator inputs. A crystal in series with a trimmer capacitor is connected between pins 12 and 13. The output of the oscillator is divided to provide the four subcarrier phases required in the encoder. The crystal frequencies are:

PAL mode 8,867238 MHz
NTSC mode 7,15909 MHz

LUMO, LUMI, pins 7 and 8.

Luminance output and input. The combined luminance and sync signal appearing at pin 7 must be d.c. coupled to pin 8 via an appropriate luminance delay line or resistor network. Resistors must have a tolerence of ± 5%, or better, as they affect the d.c. level at COVO, pin 6.

CHRBL, pin 10.

Chrominance filtering can be accomplished by connecting a chrominance frequency tuned filter (4,43 MHz or 3,57 MHZ), via a blocking capacitor to pin 10. This point is the chrominance summing junction and has a nominal internal impedance of 1,5 kΩ. If a filter is used at this point then the delay caused to the chrominance signal should be compensated by an appropriate luminance delay line.

COVO, pin 6.

Composite video output is internally buffered giving a nominal output voltage swing of 2 V sync-white and a nominal sync 5 V level.

PL/$\overline{\text{NT}}$, pin 14.

PAL/NTSC, select input selects PAL mode when HIGH and NTSC mode when LOW. This input is TTL compatable. An internal pull-up resistor selects PAL if the pin is not connected.

RAMP, pin 15.

Ramp timing component connection. A capacitor and resistor connected to pin 15 provide timing information for the colour burst and for PAL phase switching. Alternative components may be used to optimise for NTSC operation.

V_{CC}, pin 11.

12 volt supply.

GND, pin 9.

Ground connection, zero volts.

CBLNK, pin 17.

Blanking input when high, switches off colour inputs. CBLNK must be high during sync and colour burst unless colour inputs are all low at this time. This input is TTL compatible.

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Supply voltage V_{11-9}	max.	13,2	V
Voltages, pin 1,2,3,4,5,14,16,17,18	max.	V_{11-9}	V
Storage temperature		−20 to +125	°C
Operating ambient temperature		0 to + 70	°C

CHARACTERISTICS

V_{11-9} = 12 V; T_{amb} = 25 °C; measured in Fig. 3 unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{11-9}	10,8	12	13,2	V
Supply current V_{11-9} = 12 V	I_{11}	–	55	–	mA
Oscillator stability, pins 12 and 13					
Crystal type 4322 143 04051					
V_P = 10,8 to 12 V		–	+50	–	Hz
V_P = 12 to 13,2 V		–	–50	–	Hz
Digital inputs					
$\overline{CSYNC}$, CBLNK, PL/$\overline{NT}$ pins 16,17,14 R0,R1,G0,G1,B0,B1 pins 18,1,2,3,4,5					
V_{IN} (LOW)	V_{IL}	–0,5	–	0,8	V
V_{IN} (HIGH)	V_{IH}	2	–	V_{11-9}	V
Input capacitance	C_i	–	–	10	pF
Input rise and fall times $\overline{CSYNC}$, CBLNK, R0,R1,G0,G1,B0,B1 pins 16,17,18,1,2,3,4,5	t_r,t_f	–	–	200	ns
Input current d.c. for V_{IN} = 0 V	I_{IL}	–	–	–100	μA
Input current d.c. for V_{IN} = 2 V	I_{IH}	–	–	20	μA
PL/$\overline{NT}$, pin 14					
Input current d.c. for V_{IN} = 0 V	I_{IL}	–	–	–500	μA
Input current d.c. for V_{IN} = 2 V	I_{IH}	–	–	–200	μA
Composite video output, pin 6					
Output amplitude (sync tip-white)	V_{6-9} (p-p)	–	2	–	V
Sync tip level	V_{6-9}	–	5	–	V
Output load resistor	R_{6-9}	0,47	1	–	kΩ
Variation of output amplitude T_{amb} = 0 to +70 °C	$V_{(p-p)}$	–	–	tbf	%
Over supply range V_{11-9} = 10,8 to 13,2 V	ΔV	–	–	tbf	%
Output impedance (with 1 kΩ load)	R_L	–	15	–	Ω
Residual chrominance on white	ΔV_{rms}	–	30	–	mV
Tolerance on luminance amplitude	ΔV	–	10	–	%
Tolerance on chrominance amplitude	ΔV	–	10	–	%
Tolerance on chrominance phase	ΔQ	–	tbf	–	%
Chrominance band limiting, pin 10					
Internal resistance	R_{10-11}	–	1,5	–	kΩ
Luminance delay, pins 7 and 8					
Nominal series resistor (±5%)	R_S	–	1,2	–	kΩ
Nominal load resistor at luminance input (±5%)	R_L	–	1	–	kΩ
Ramp timing, pin 15 (see Fig. 4)					
With external RC circuit R = 36 kΩ; C = 330 pF (note 1)					
Start of burst from line sync	t_b	–	5,7	–	μs
Burst width	t_w	–	2,5	–	μs
Threshold for seperation of equalizing pulses and sync pulses	t	36	44	56	μs

Note: 1. A figure of 5 pF is assumed for external capacitance. This figure includes temperature dependence of the components.

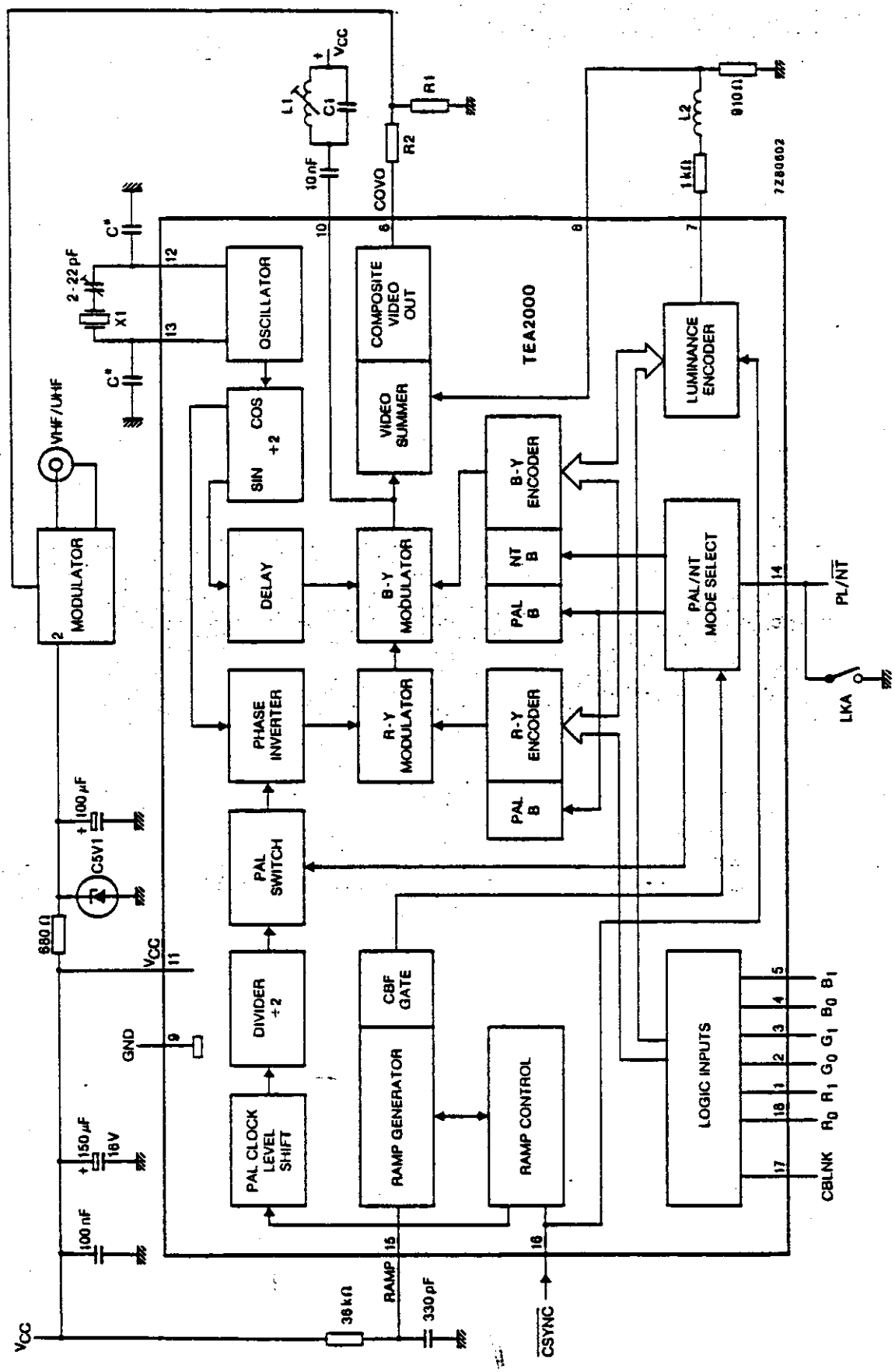

Fig. 2 Internal circuit details and typical external connections.

X1 (PAL) = 8,867238 MHz
X1 (NTSC) = 7,159100 MHz
C* = 5,6 pF only for mask version 1

COMPONENT	PAL	NTSC
L1	15 μH	18 μH
C1	82 pF	100 pF
L2	DL270	DL330
R1	430 Ω	510 Ω
R2	510 Ω	750 Ω
M1	UM1233	UM1622
LKA	o/c	made

Component list for Fig. 2.

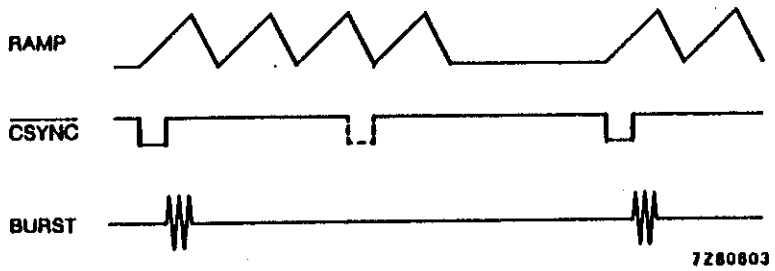

Fig. 3 Ramp timing.